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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/086,376	03/04/2002	Michihiro Horiuchi	TAMA.0001	2698

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EXAMINER	
FAROOQ, MOHAMMAD O	
ART UNIT	**PAPER NUMBER**
2182	

DATE MAILED: 01/21/2004.

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/086,376	HORIUCHI ET AL.	
	Examiner	Art Unit	
	Mohammad O. Farooq	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12 and 15-22* is/are rejected.

7)☒ Claim(s) *13 and 14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

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PRIMARY EXAMINER
GROUP 2100

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1, 2, 7-12 and 15-22are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al., U.S. Pat. No. 5,050,165 in view of Newman, U.S. Pat. No. 5,287,452.

2. Claims 3-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al., U.S. Pat. No. 5,050,165 in view of Newman, U.S. Pat. No. 5,287,452 further in view of Downey, U.S. Pat. No. 4,918,647.

3. As to claim 1, Yoshioka et al. teach a data processor comprising:

a central processing unit (item 61, fig. 1);

a data transfer control circuit (decision circuit; items 33, 36, fig. 1) for controlling data transfers under control of said central processing unit; and

a peripheral circuit (memory control circuit; item 51, fig. 1; fig. 6; fig. 7), for requesting data transfers,

wherein said peripheral circuit selects (via selector; item 71, fig. 6) one of the input terminals thereof, processes input data from the selected input terminal, requests the transfer of the processing result, and outputs identification information which permits the identification of the selected input terminal (col. 6, line 60- col. 7, line17), and

said data transfer control circuit has destination address register with variable bits (col. 11, line 65- col. 12, line 2).

Yoshioka et al. do not teach low-order bits variable with identification information from peripheral circuit. Newman teaches low-order bits variable with identification information from peripheral circuit (col. 7, lines 14-27). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Yoshioka et al. and Newman because that would provide simultaneous update data/memory without extra operations of the system (col. 2, liens 23-40).

4. As to claim 2, Yoshioka et al. teach wherein said peripheral circuit comprises a data register (buffer memory; item 219, fig. 8) shared for storing the processing results of input data.

5. As to claim 3, neither Yoshioka et al. nor Newman teach peripheral circuit is an analog-to-digital circuit having converter section and a converter control section, said converter section comprising plurality of input channels, conversion data register for storing conversion results; and said converter control section requests stored data stored in conversion data register and outputting code information which permits the identification of analog input channels corresponding to said conversion results.

Downey teaches peripheral circuit is an analog-to-digital circuit having converter section and a converter control section (see items 13, 14, fig. 2 and fig. 3), said converter section comprising plurality of input channels (see fig. 2 and fig. 3), conversion data register for storing conversion results (item 14, fig. 2); and said converter control section requests stored data stored in conversion data register and outputting code information which permits the identification of analog input channels corresponding to said conversion results (inherent; see fig. 2 and fig. 3). However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of Yoshioka et al. and Newman with Downey because that would provide fixed and unchanged control signals for digitized data/signals from analog input (col. 2, lines 16-32).

6. As to claims 4-6, neither Yoshioka et al. nor Newman teach converter section further comprises an analog multiplexer for selection of input channels, a channel-select register for holding selection information and a computing element.

Downey teaches converter section further comprises an analog multiplexer for selection of input channels (item 12, fig. 2 and fig. 3), a channel-select register (sample and hold circuits; item 11, fig. 2 and fig. 3) for holding selection information and a computing element (counter/timer unit; item 22, fig. 4A). However, it would have been obvious to one of ordinary skill in the art at the time of invention to modify the combination of Yoshioka et al. and Newman with Downey because that would provide the system to receive and store the signals/data for controlling the operation of the circuit (abstract).

7. As to claims 7 and 8, Yoshioka et al. teach destination address register thereof according to the loading transfer control conditions can be overwritten (rewritten) with said identification information (since variable bit-length allotted to destination address; col. 11, lines 65- col. 12, line 2).

8. As to claim 9, Yoshioka et al. do not teach system comprising a RAM.

Newman teaches system comprising a RAM (item 198, fig. 2). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Yoshioka et al. and Newman because that would provide a manner as to not interfere with the access to the system memory by the CPU (col. 2, lines 23-40).

9. As to claim 10, Yoshioka et al. teach the data processor is formed into a single semiconductor chip (bridge circuit; item 3, fig. 1).

10. As to claim 11, Yoshioka et al. teach a data processor comprising:

a central processing unit (item 61, fig. 1);

a data transfer control circuit (decision circuit; items 33, 36, fig. 1) for controlling data transfers under control of said central processing unit; and

a peripheral circuit (memory control circuit; item 51, fig. 1; fig. 6; fig. 7), for requesting data transfers,

wherein said peripheral circuit performs (via selector; item 71, fig. 6) processing in response to the occurrence of an event (or input) to be dealt with, requests the transfer of the processing result, and outputs identification information which permits the identification of the event occurrence corresponding to the processing result (or the input channels, per applicants' specification; col. 6, line 60- col. 7, line17), and

said data transfer control circuit comprises a destination address register with variable bits (col. 11, line 65- col. 12, line 2).

Yoshioka et al. do not teach low-order bits variable with identification information from peripheral circuit. Newman teaches low-order bits variable with identification information from peripheral circuit (col. 7, lines 14-27). However, it would have been obvious to one of ordinary skill in the art at the time of invention to combine the teachings of Yoshioka et al. and Newman because that would provide simultaneous update data/memory without extra operations of the system (col. 2, liens 23-40).

11. As to claims 20 and 22, Yoshioka et al. teach wherein said peripheral circuit has a plurality of data registers (buffer memory; item 219, fig. 8) for storing the processing results of input data from said data input channels.

12. Claims 12, 15-18 and 19 have similar limitations as claims 2, 7-10 and 1 respectively. Yoshioka et al. and Newman in combination teach apparatus as set forth in claims 2, 7-10 and 1. Therefore, Yoshioka et al. and Newman in combination also teach apparatus as set forth in claims 12, 15-18 and 19.

13. Claim 21 has similar limitations as claim 11. Yoshioka et al. and Newman combination teach apparatus as set forth in claim 11. Therefore, Yoshioka et al. and Newman in combination also teach apparatus as set forth in claim 21.

Allowable Subject Matter

14. Claims 13 and 14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mohammad O. Farooq whose telephone number is (703) 305-3888. The examiner can normally be reached on 8:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

FRITZ FLEMING
PRIMARY EXAMINER
GROUP 2100

Mohammad O. Farooq
January 14, 2004